Lesson plan

Name of the faculty : Dr. Umesh Gupta

Discipline : Electrical & Electronics Engineering

Semester : 6th

Subject : VLSI Design

Lesson Plan Duration : 15 weeks (From January, 2020 to April 2020)

Work Load (Lecture/ Practical) per week (in hours): Lecture-02, Practical-01

Week	Theory		Practical	
	Lecture day	**Topic(Including assignment/test)**	**Practical Day**	**Topic**
1st	1st	A BASIC MOS TRANSISTOR : Enhancement mode & Depletion mode	1st	Design of Half-Adder, Full Adder, Half Subtractor, Full Subtractor
	2nd	Fabrication (NMOS, PMOS, CMOS, BiCMOS) Technology		
2nd	1st	NMOS transistor current equation	2nd	Design a parity generator
	2nd	Second order effects – MOS Transistor Model		
3rd	1st	NMOS & CMOS INVERTER	3rd	Design a 4 Bit comparator
	2nd	GATES : NMOS & CMOS inverter		
4th	1st	Determination of pull up / pull down ratios	4th	Design a RS & JK Flip flop
	2nd	Stick diagram – Lamda based rules		
5th	1st	Super buffers – BiCMOS & steering logic	5th	Design a 4: 1 Multiplexer
	2nd	SUB SYSTEM DESIGN & LAYOUT		
6th	1st	Structured design of combinational circuits	6th	Design a 4 Bit Up / Down Counter with Loadable Count
	2nd	Dynamic CMOS & clocking		

7th	**Sessional -I Examination+Activity**			
8th	1st	Tally circuits – (NAND-NAND	8th	Design a 8 bit shift register
	2nd	NOR-NOR and AOI logic		
9th	1st	EXOR structure	9th	Design a arithmetic unit
	2nd	Barrel shifter		
10th	1st	DESIGN OF COMBINATIONAL ELEMENTS	10th	Implement ADC & DAC interface with FPGA
	2nd	REGULAR ARRAY LOGIC : NMOS PLA		
11th	1st	Programmable Logic Devices	11th	Implement a serial communication interface with FPGA
	2nd	Finite State Machine PLA		
12th	1st	Introduction to FPGA	12th	Implement a Telephone keypad interface with FPGA
	2nd	VHDL PROGRAMMING: RTL Design		
13th	1st	Combinational logic – Types – Operators	13th	Implement a VGA interface with FPGA
	2nd	Packages – Sequential circuit		
14th	1st	Sub-programs – Test benches. (Examples: address	14th	Implement a PS2 keypad interface with FPGA
	2nd	counters, flipflops FSM, Multiplexers / De-multiplexers		
15th	1st	Revision	15th	Implement a 4 digit seven segment display
	2nd	Revision		
16th	**Sessional -II Examination+Activity**			

Faculty Signature